What is claimed is:

1. A method for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the method comprising:

applying an electric field to the die via a voltage-application tool, separate from the die and using the applied electric field to stimulate circuitry in the die;

detecting a response of dic to the applied electric field; and

using the response to detect an electrical characteristic from the die.

2. The method of claim 1, wherein applying an electric field includes applying an electric field to circuitry via a die passivation layer in a conventionally packaged semiconductor die.

3. The method of claim 1, wherein applying an electric field includes applying an electric field to circuitry via a backside of a flip-chip packaged die.

4. The method of claim 3, wherein applying an electric field to circuitry via a backside of a flip-chip packaged die includes applying an electric field via a thinned backside of the flip-chip packaged die.

5. The method of claim 4, further comprising thinning the backside of the flip-chip packaged die and thereby forming the thinned backside.

6. The method of claim 1, wherein applying an electric field includes applying an electric field to circuitry via an insulator portion of silicon-on-insulator structure in a die.

7. The method of claim 6, further comprising thinning a portion of the die and exposing the insulator portion of the silicon-on-insulator structure, wherein applying an electric field to circuitry via the insulator portion includes applying the electric field via the exposed insulator portion.

8. The method of claim 1, wherein applying the electric field includes using at least one of: a scanning probe microscope, and atomic force microscope and a capacitance probe microscope.

9. The method of claim 1, wherein applying an electric field to the die includes positioning a probe tip over a portion of circuitry in the die and applying a voltage to the probe tip.

10. The method of claim 9, wherein applying a voltage to the probe tip includes applying a voltage that varies over time to the probe tip.

11. The method of claim 9, wherein detecting a response of the die to the applied electric field includes detecting a position of the probe tip over the die and mapping the detected response to circuitry in the die below the probe tip.

12. The method of claim 9, wherein positioning the probe tip includes scanning the probe tip over the die.

13. The method of claim 12, wherein detecting a response of the die includes detecting responses from a plurality of circuits in the die as the probe tip is scanned over the circuits.

14. The method of claim 9, wherein applying a voltage to the probe tip includes applying a periodic voltage that is relative to a voltage at a reference node in the die.

15. The method of claim 9, wherein positioning a probe tip includes positioning a probe tip having a radius that is sufficiently small to stimulate a selected node in the die without necessarily stimulating circuitry adjacent to the selected node.

16. The method of claim 9, wherein positioning a tip over a portion of circuitry in the die includes positioning the tip using nanometer-level resolution.

17. The method of claim 1, wherein applying an electric field includes applying the electric field to circuitry via an opaque layer in the die, the circuitry being buried in the die below the opaque layer.

18. The method of claim 1, further comprising using the detected electrical characteristic to provide a modified die design and manufacturing a semiconductor device using the modified die design.

19. A semiconductor device manufactured using the modified die design of claim 18.

20. The method of claim 1, further comprising using the detected electrical characteristic to modify a manufacturing process for the die and subsequently using the modified manufacturing process to manufacture additional dies.

21. A method for analyzing and repairing a semiconductor die having silicon-on-insulator structure, the method comprising:

applying an electric field to the die via the insulator portion of the SOI structure using a probe tip and using the applied electric field to switch a non-functioning transistor in the die between a passing state and a blocking state;

detecting the switching of the non-functioning transistor and identifying the location of the non-functioning transistor as a function of the location of the probe tip when the switching is detected; and

repairing the non-functioning transistor.

22. The method of claim 21, wherein using the applied electric field to switch a non-functioning transistor includes switching a transistor having at least one of: an oxide short and an open gate.

23. The method of claim 21, wherein repairing the non-functioning transistor comprises depositing a gate on the SOI structure at the location of the probe tip when the non-functioning transistor is switched, the gate being adapted to switch the transistor between a passing state and a blocking state.

24. The method of claim 23, further comprising electrically coupling the gate to other circuitry in the die.

25. The method of claim 23, further comprising:

re-applying an electric field to the die via the insulator portion of the SOI structure using a probe tip and using the applied electric field to switch a second non-functioning transistor in the die between a passing state and a blocking state; and

detecting the switching of the second non-functioning transistor and identifying the location of the second non-functioning transistor as a function of the location of the probe tip when the switching is detected.

26. The method of claim 23, wherein depositing a gate includes using a focused ion beam (FIB) to deposit a gate.

27. The method of claim 21, after repairing the non-functioning transistor, further comprising:

applying an electric field to the die and using the applied electric field to stimulate circuitry in the die;

detecting a response of die to the applied electric field; and

using the response to detect an electrical characteristic of the die.

28. A system for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the system comprising:

means, separate from the die and adapted for applying an electric field to the die and using the applied electric field to stimulate circuitry in the die;

means for detecting a response of die to the applied electric field; and

means for using the response to detect an electrical characteristic of the die.

29. A system for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the system comprising:

a probe tip arrangement, separate from the die and adapted for applying an electric field to the die for stimulating circuitry in the die;

electrical detection circuitry adapted for detecting a response of die to the applied electric field; and

a computer arrangement adapted for using the response to detect an electrical characteristic of the die.

30. The system of claim 29, wherein the probe tip is sufficiently small to apply an electric field to stimulate a selected circuit node in the die without necessarily stimulating surrounding circuitry in the die.